



IBM 5120  
Computing System Logic Manual

SY34-0193-0

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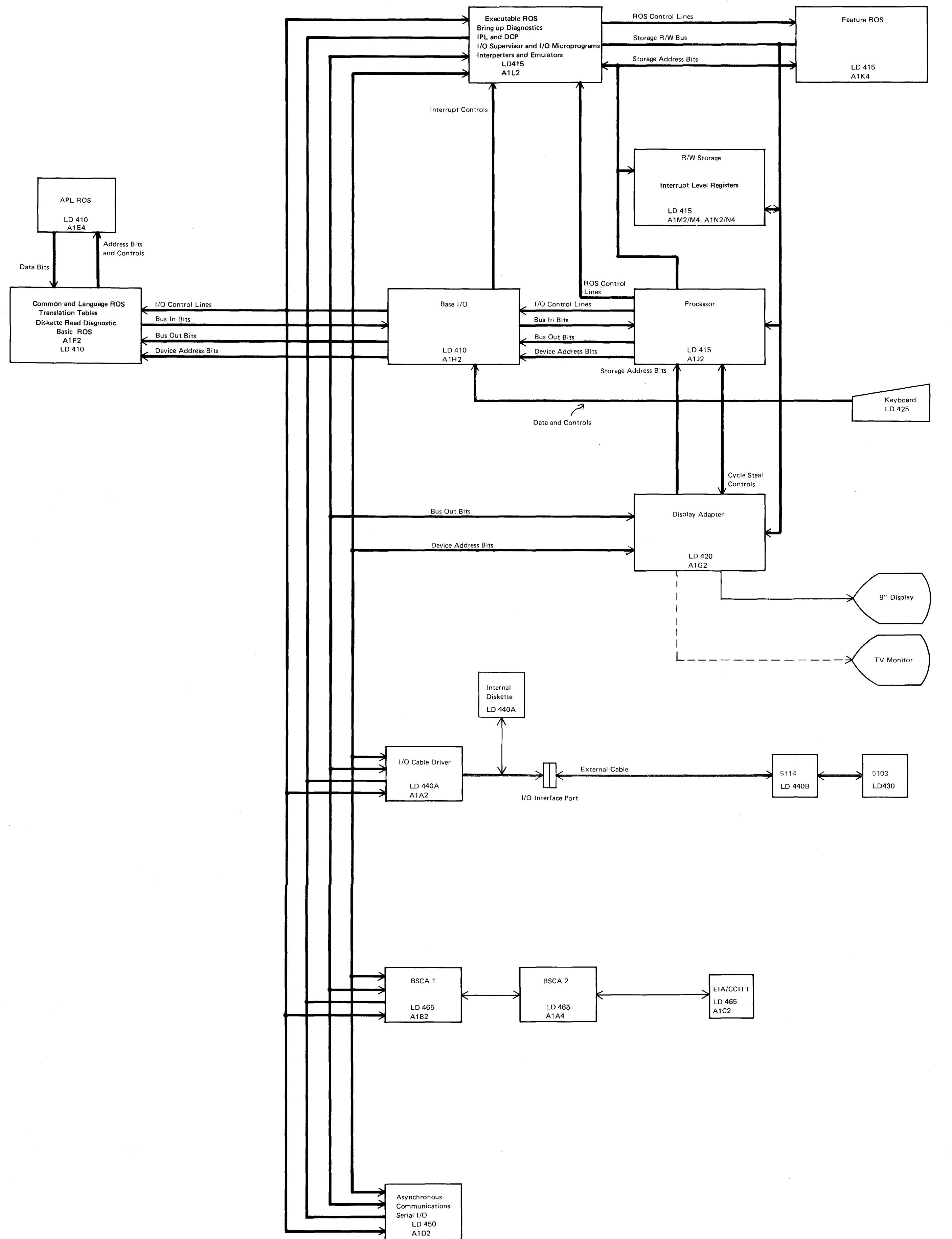
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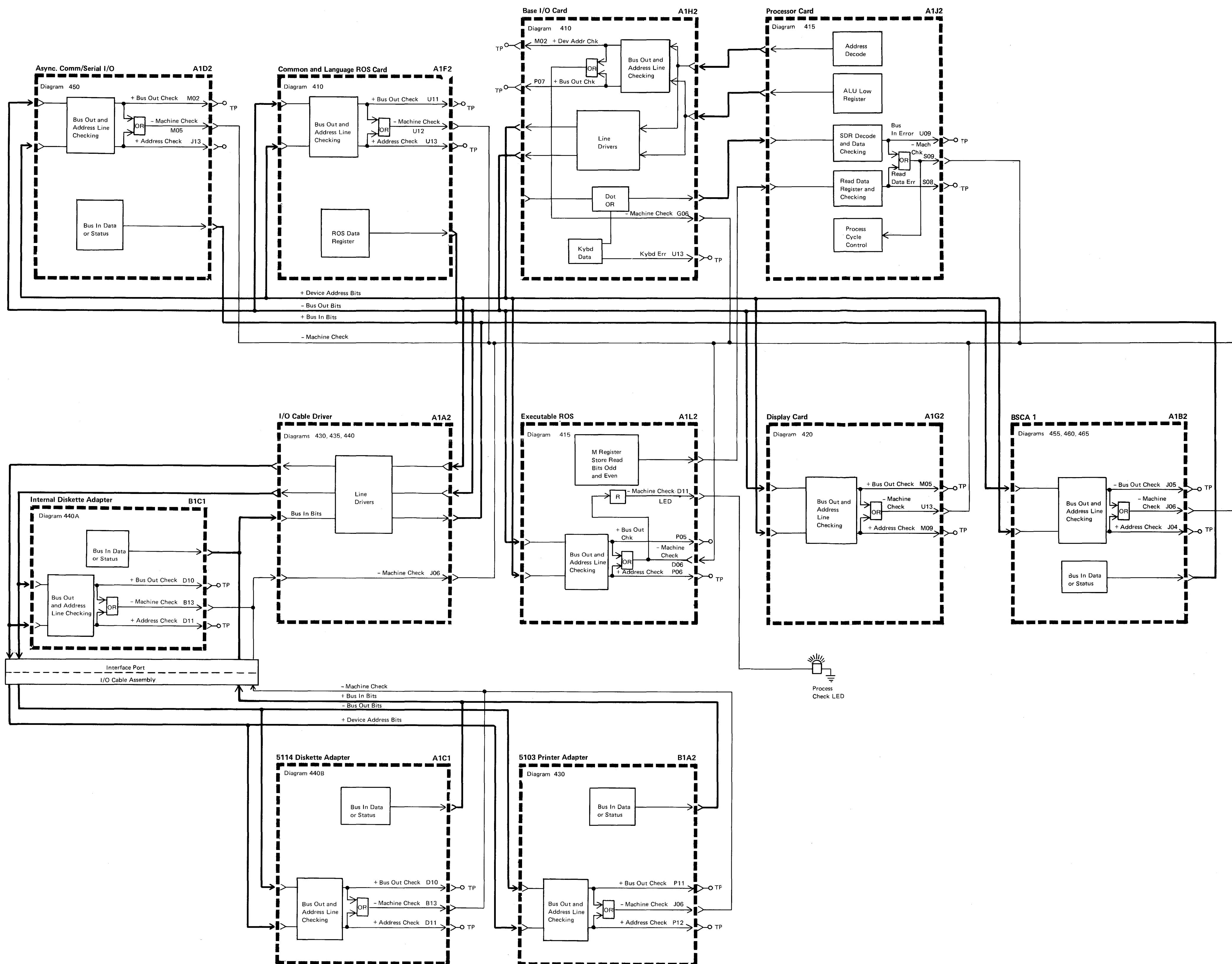
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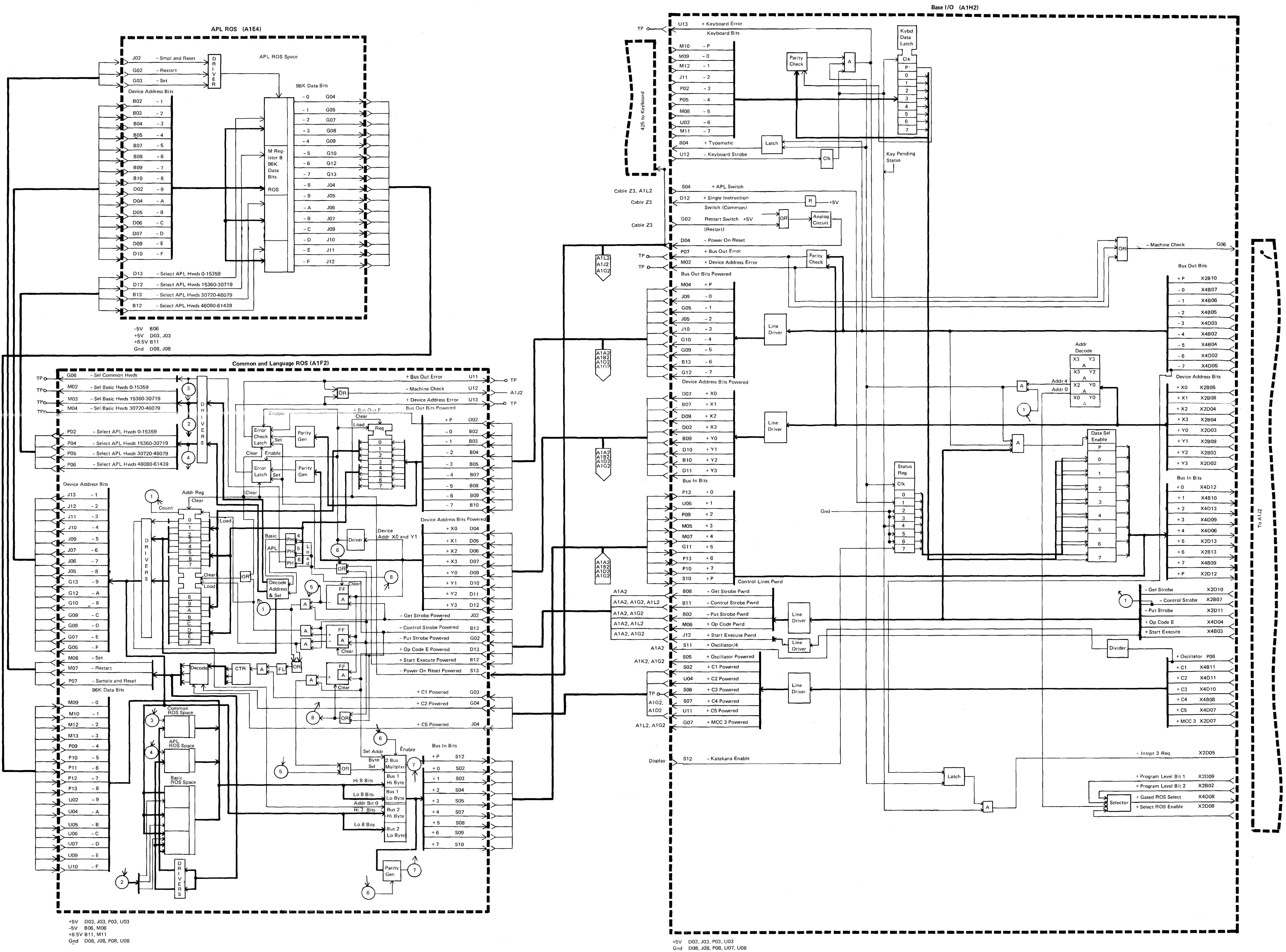


## Data Flow 400

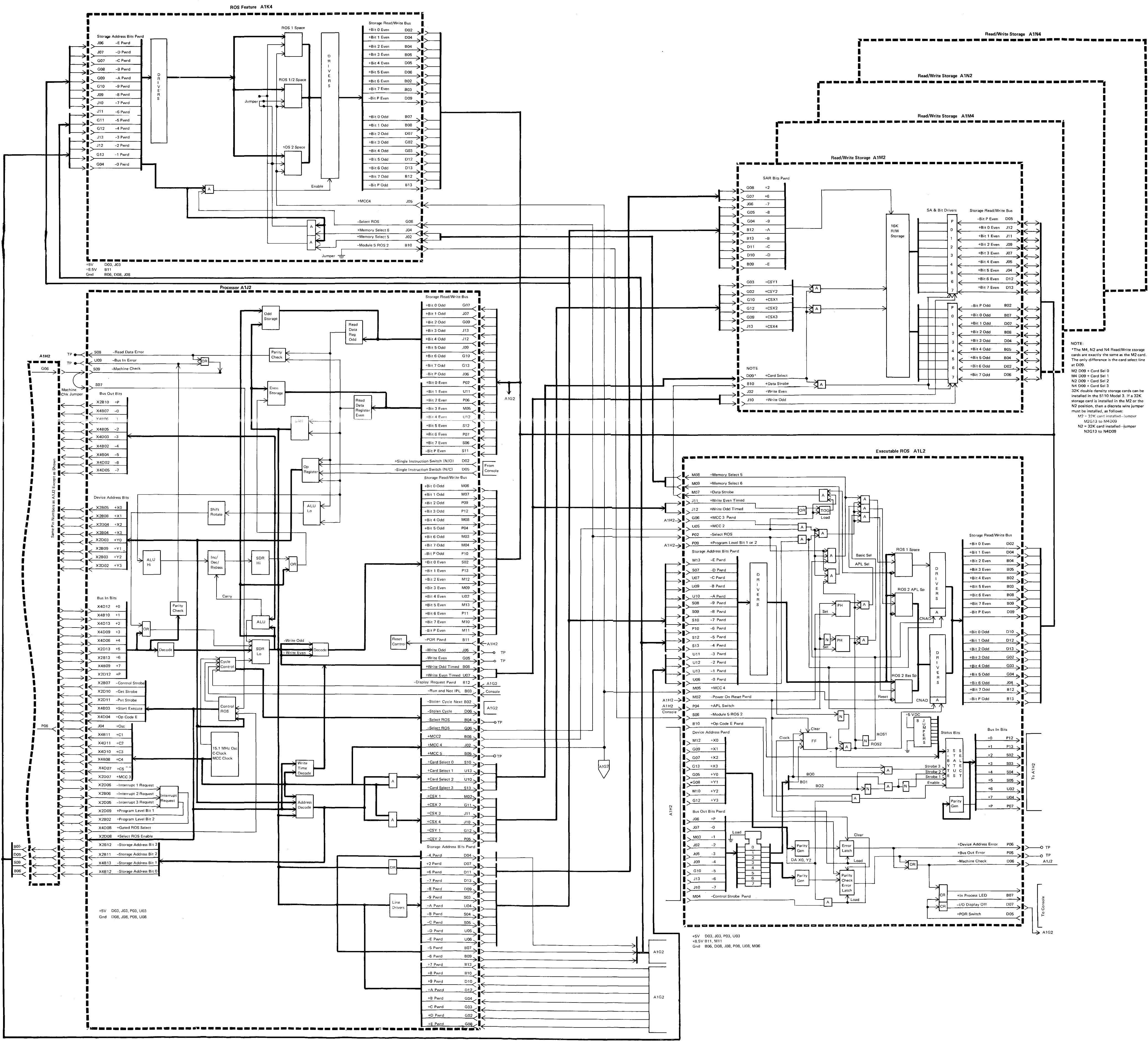


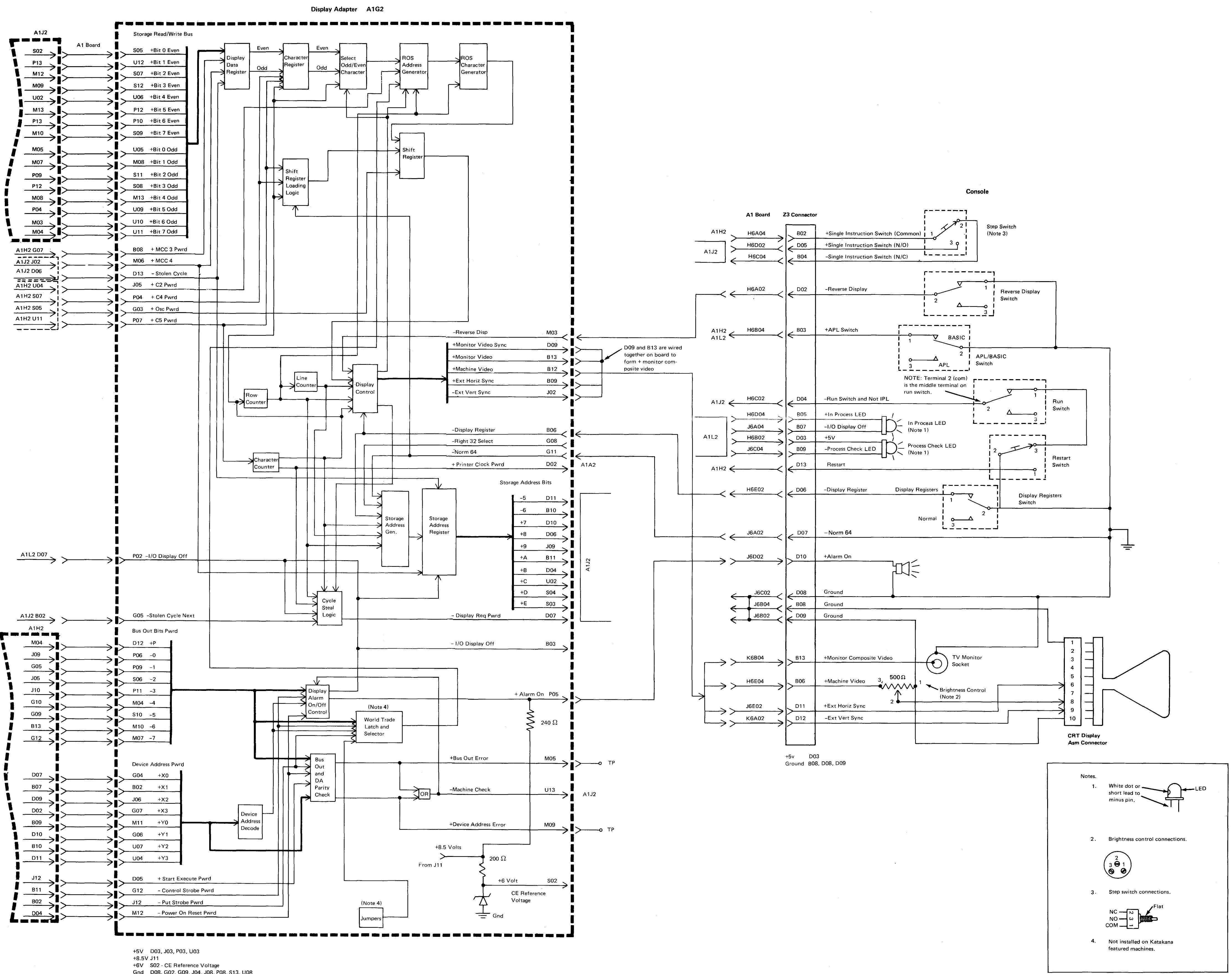
Process Check Chart 405

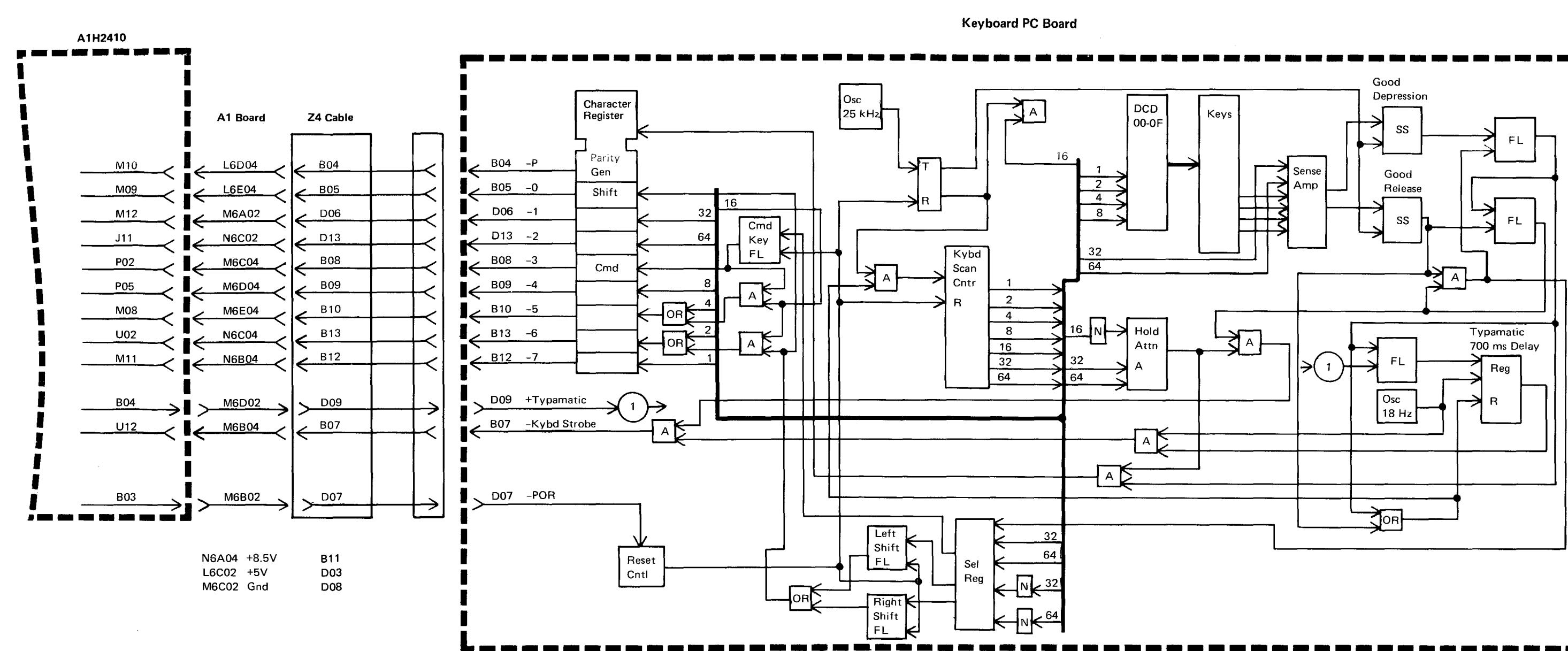
Bus Out Parity Check	D10	D10	P11	J05	M02	U11	M05	P07	U09	P05
Address Check	D11	D11	P12	J04	J13	U13	M09	M02	S08	P06
Keyboard Parity Error							U13			



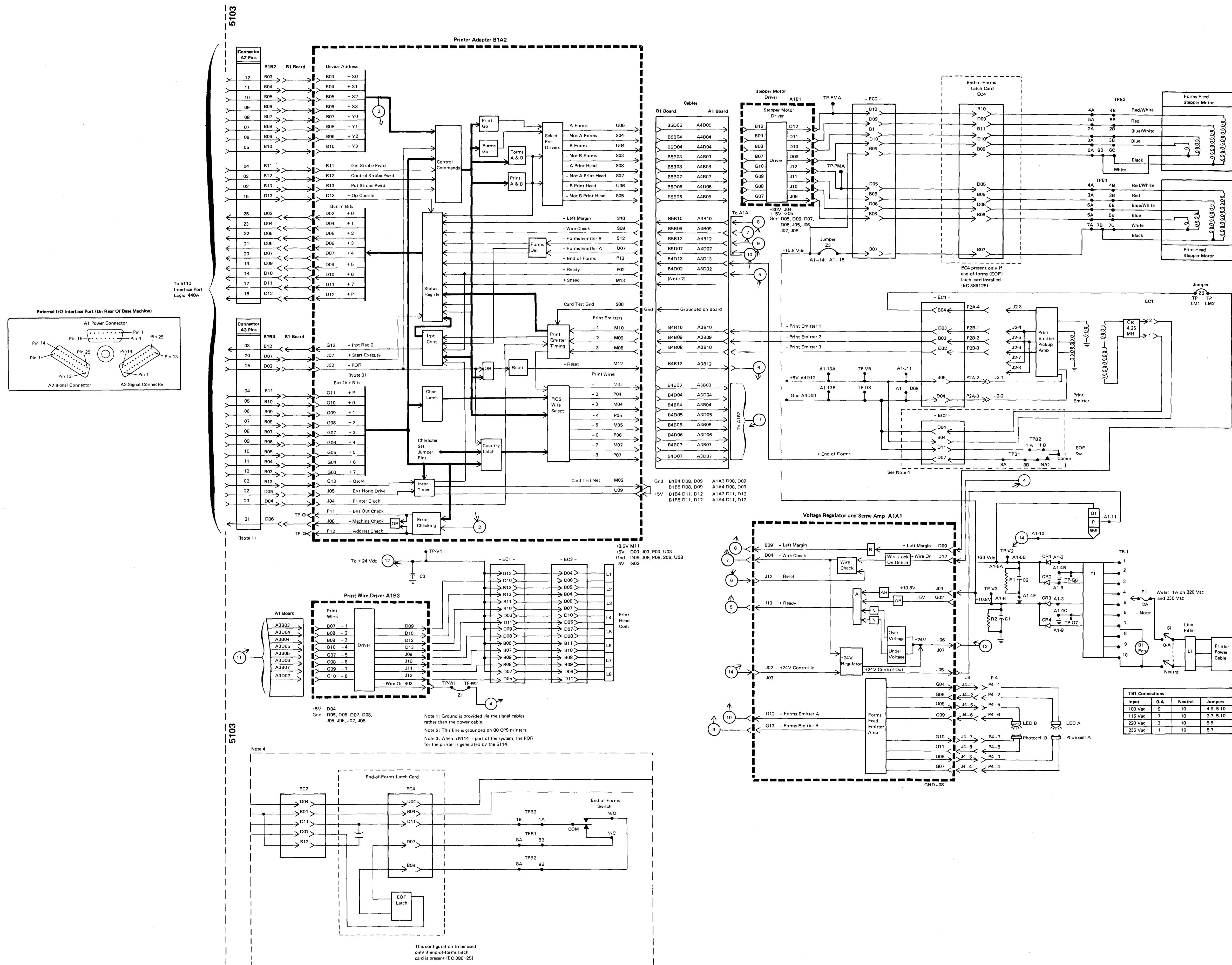
Base I/O 410  
APL ROS  
Common/Language ROS



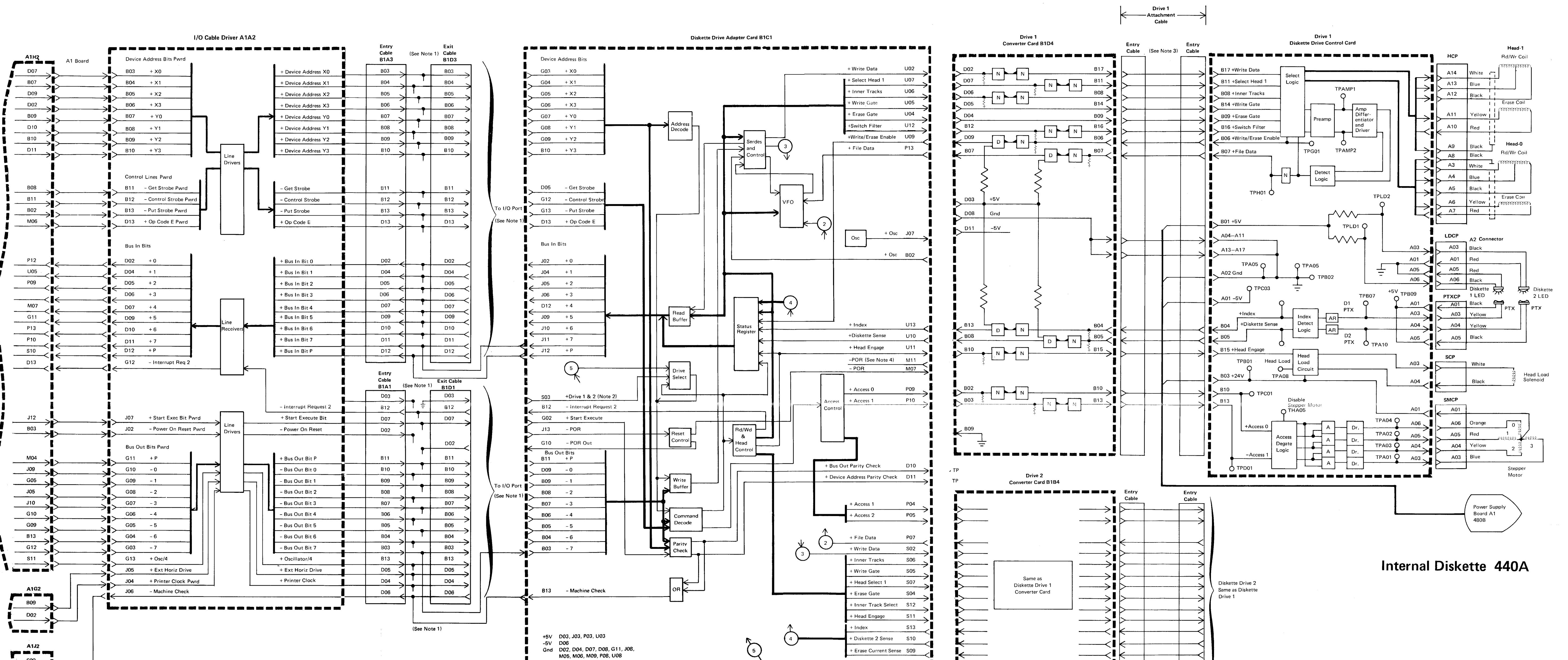




## Keyboard 425

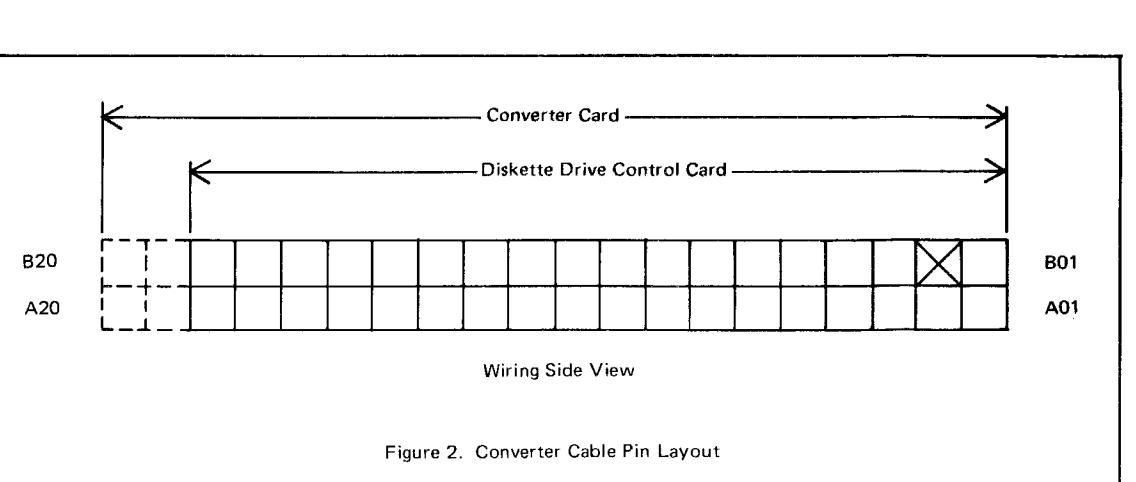
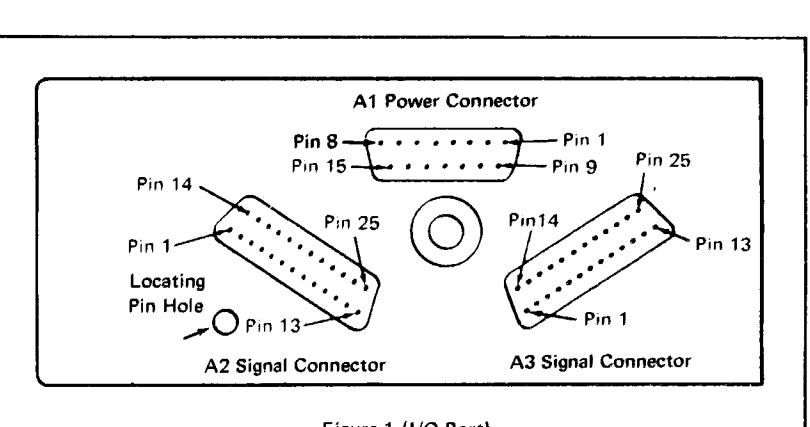


5103 Printer 430

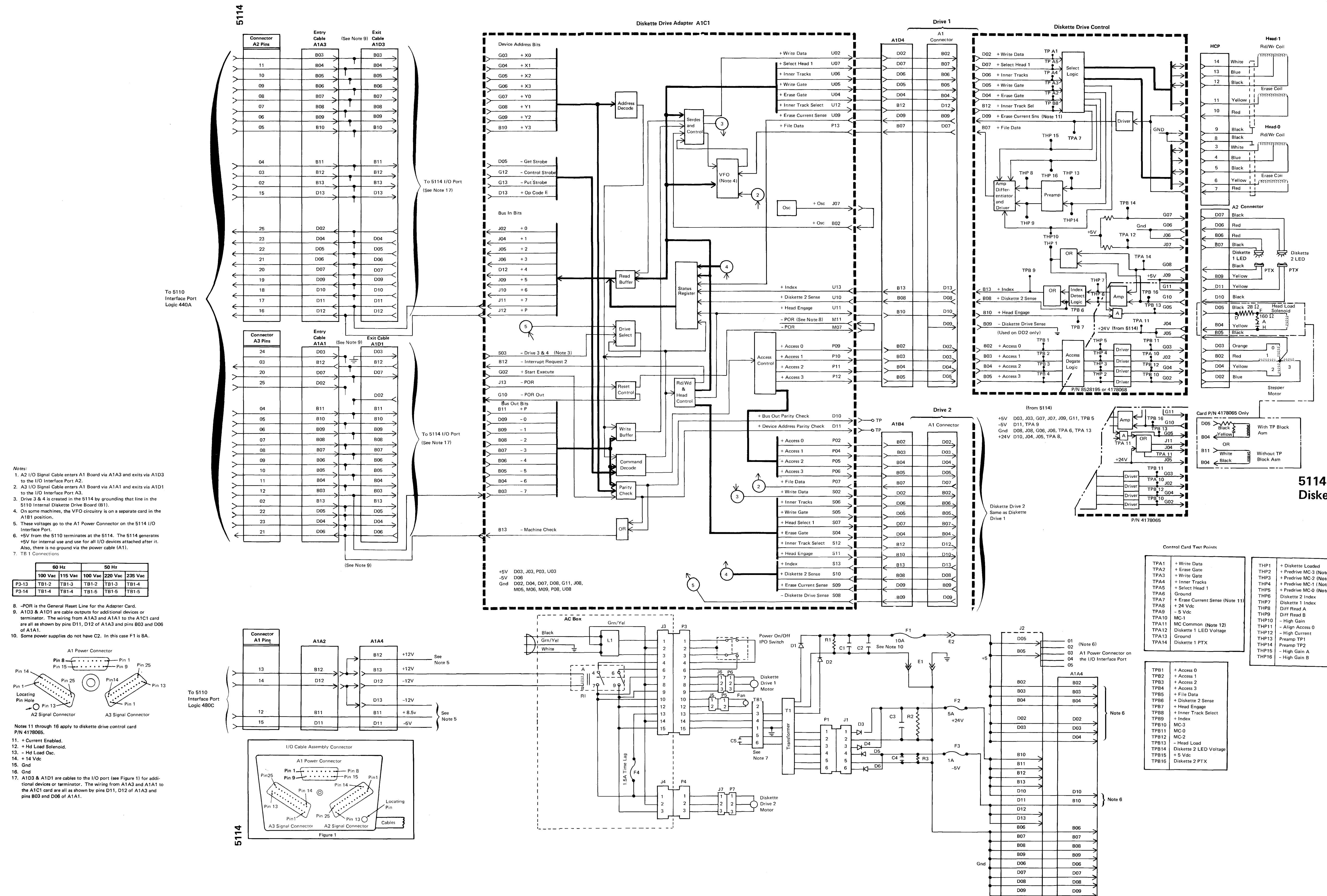


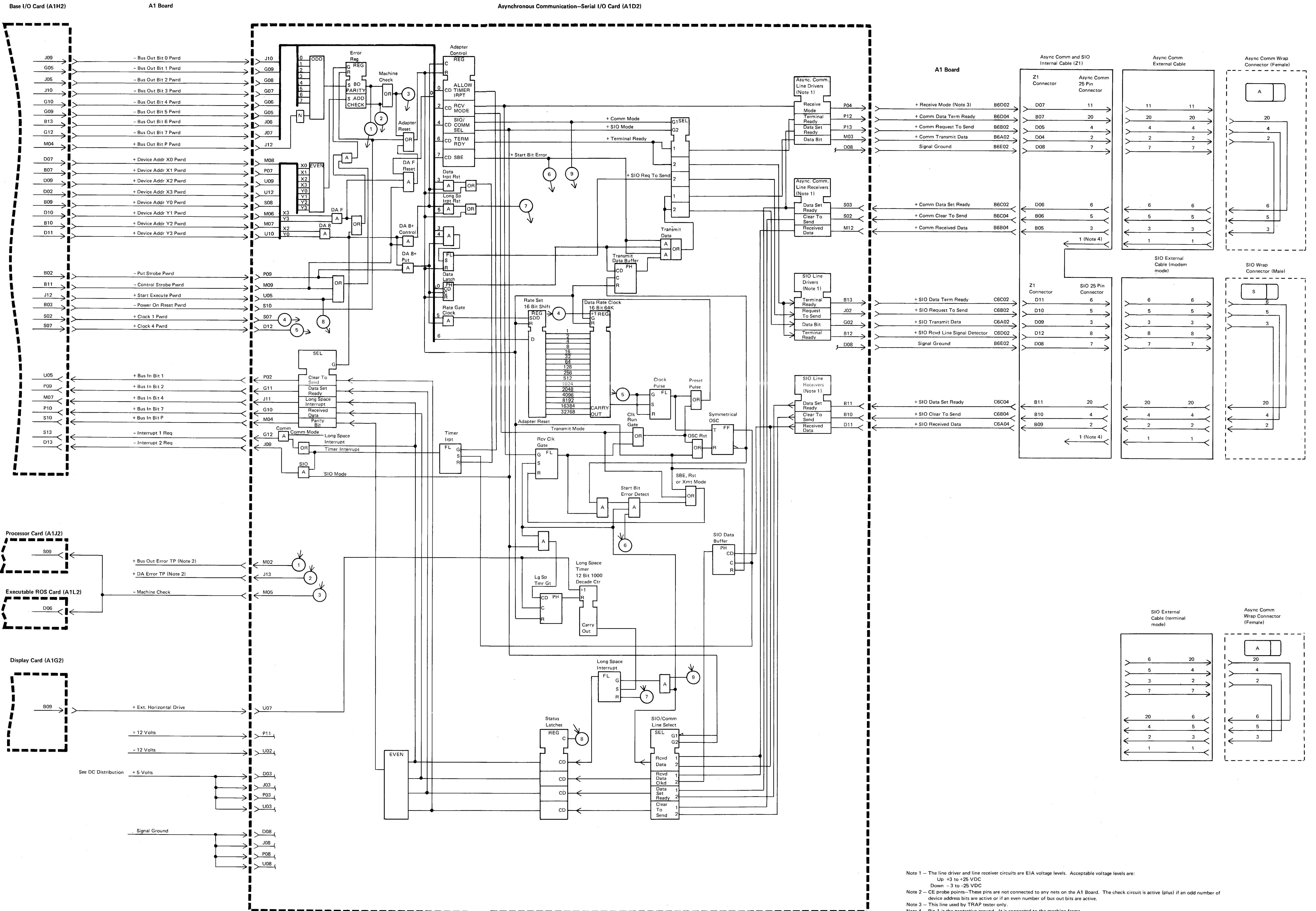
**Notes:**

- B1A3 & B1D1 are cables to the I/O port (see figure 1) for additional devices or terminator. The wiring from B1A3 and B1A1 to the B1C1 card are all as shown by pins D11, D12 of B1A3 and pins B03 and D06 of B1A1.
- This line is always floating for drive 1 and 2.
- Attachment cable pin layout (see figure 2).
- POR is the General Reset line for the Adapter Card.

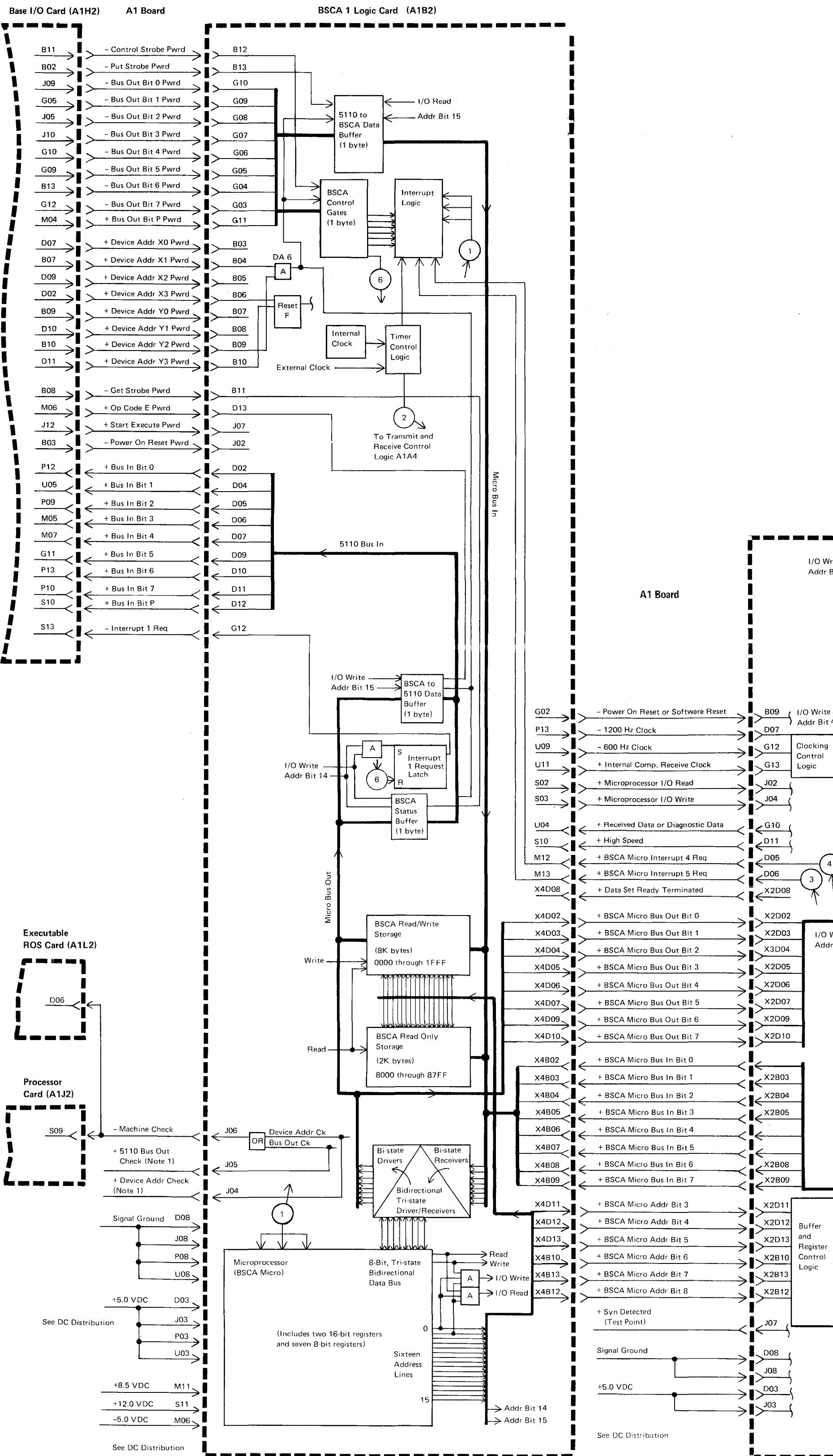


# 5114 440B Diskette Unit





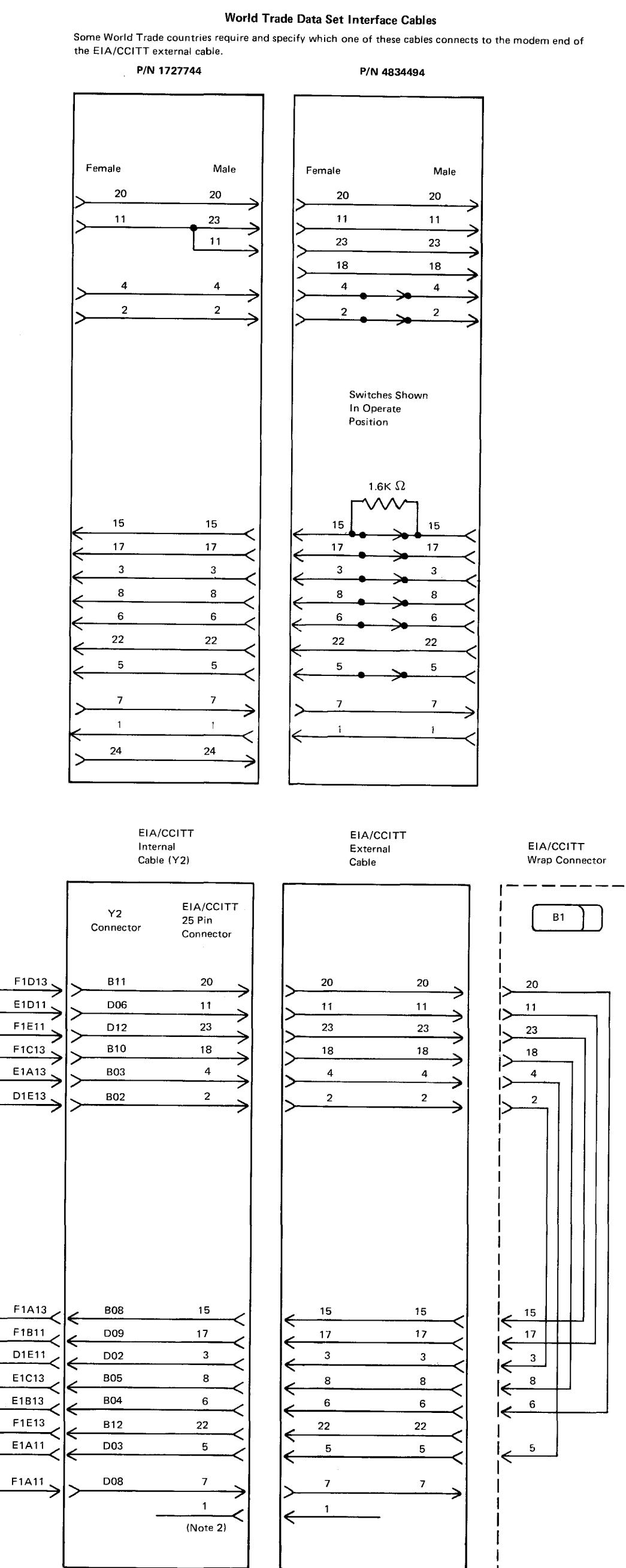
**Serial I/O** **450**  
**Synchronous Communications**



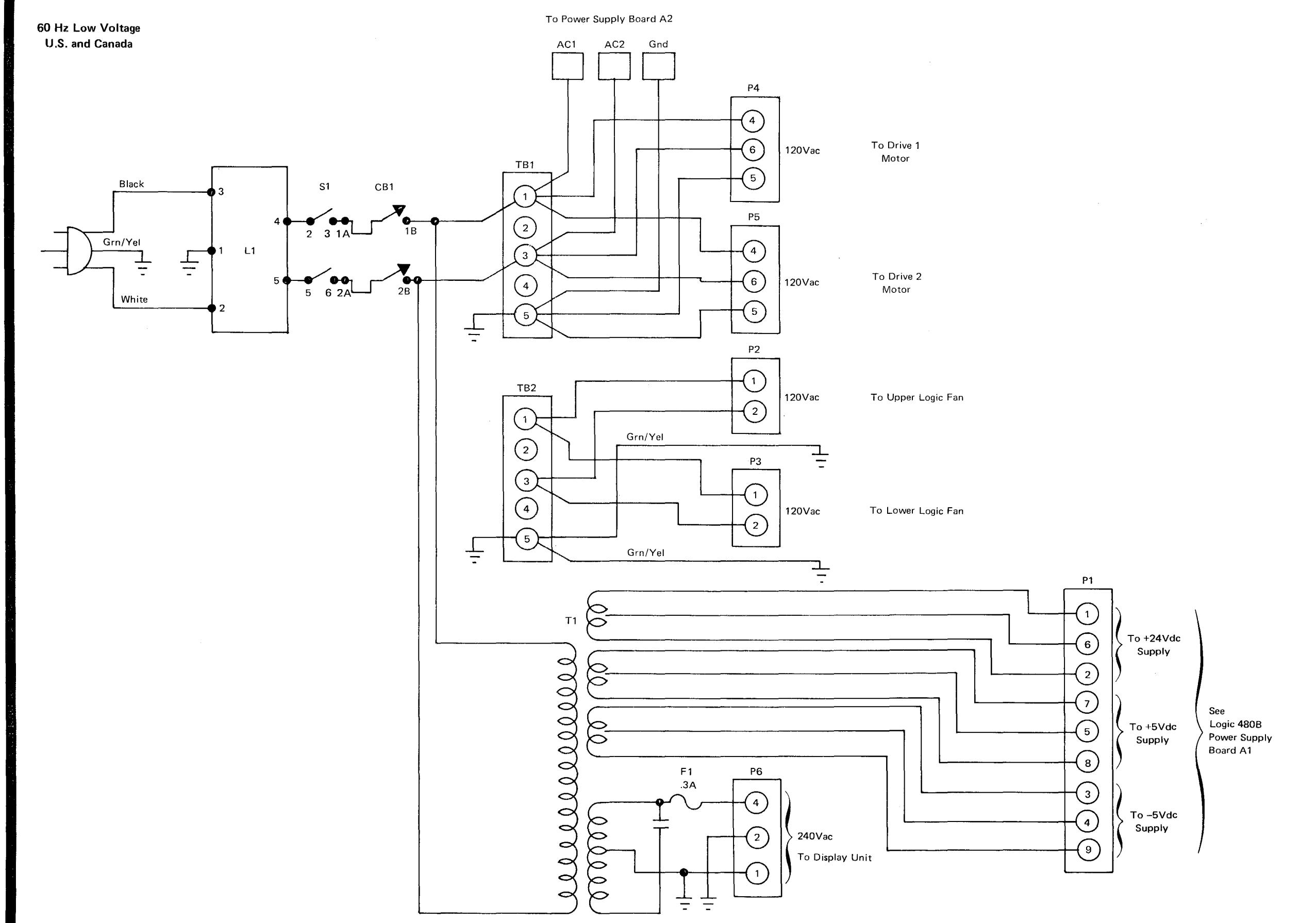
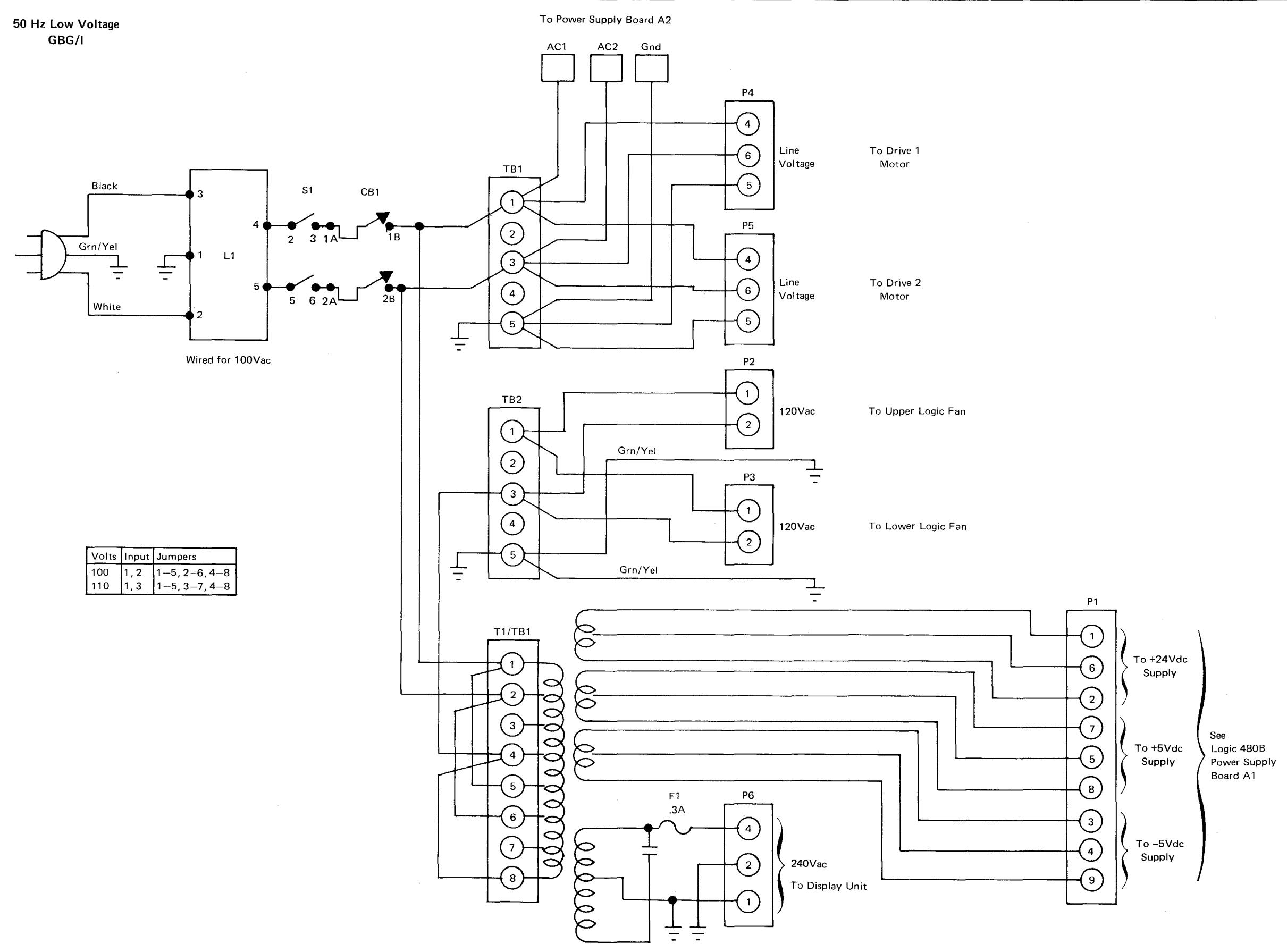
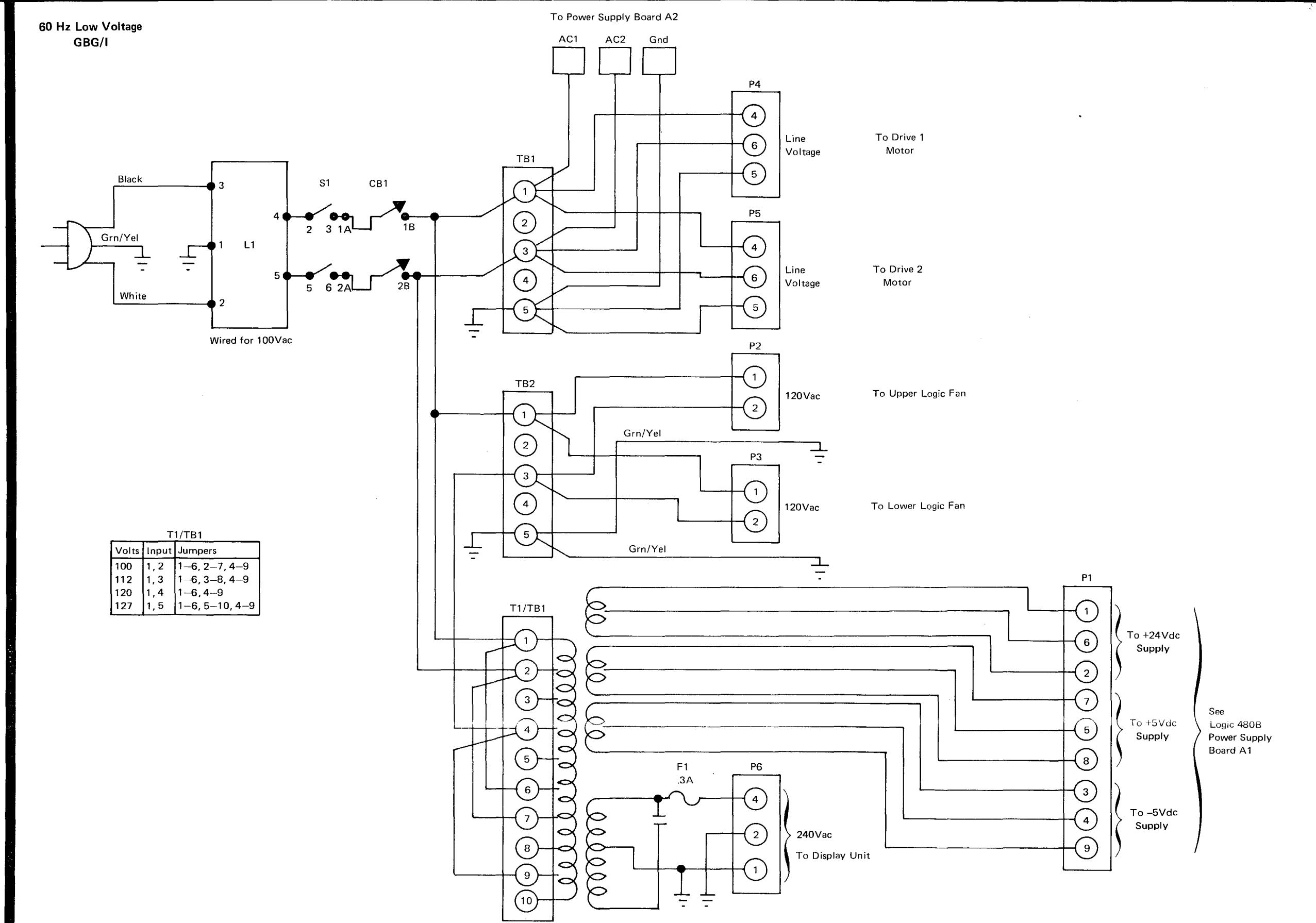
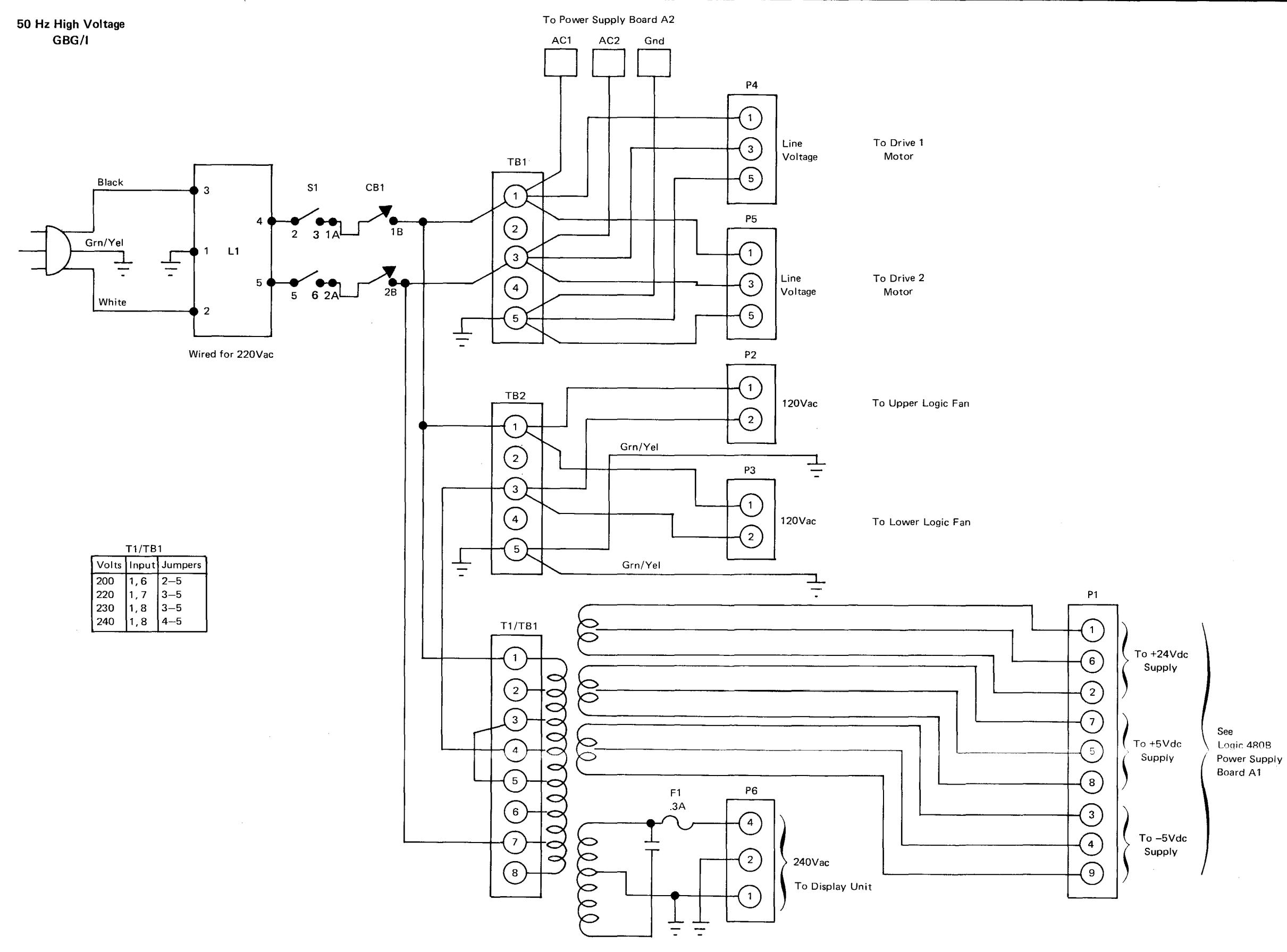
Note 1 — CE probe points — These pins are not connected to any nets on the A1 Board. The check circuit is active (plus) if an odd number of device address bits are active or if an even number of bus out bits are active.

Note 2 — Pin 1 is the protective ground. It is connected to the machine frame.

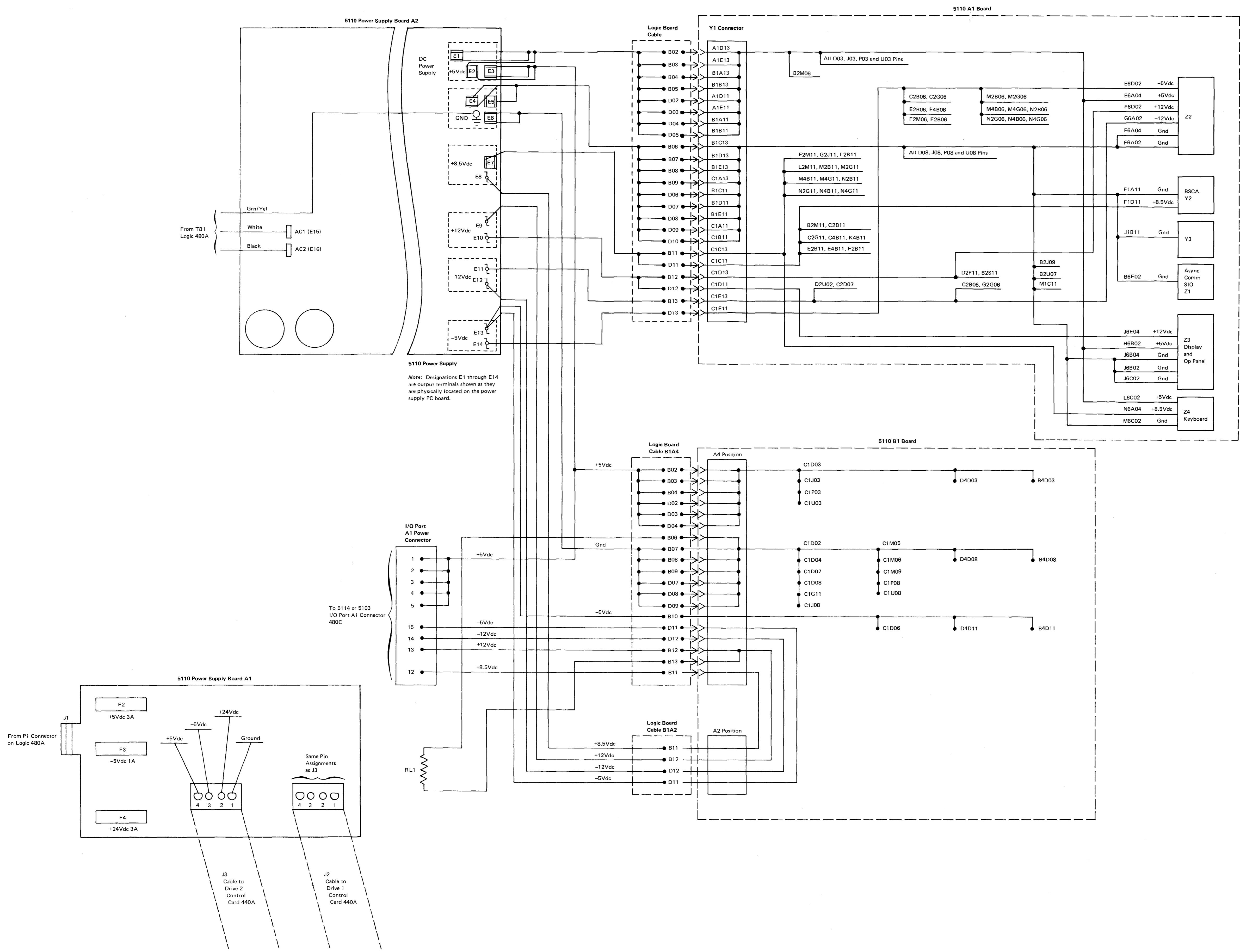
Note 3 — Used by TRAP tester only.

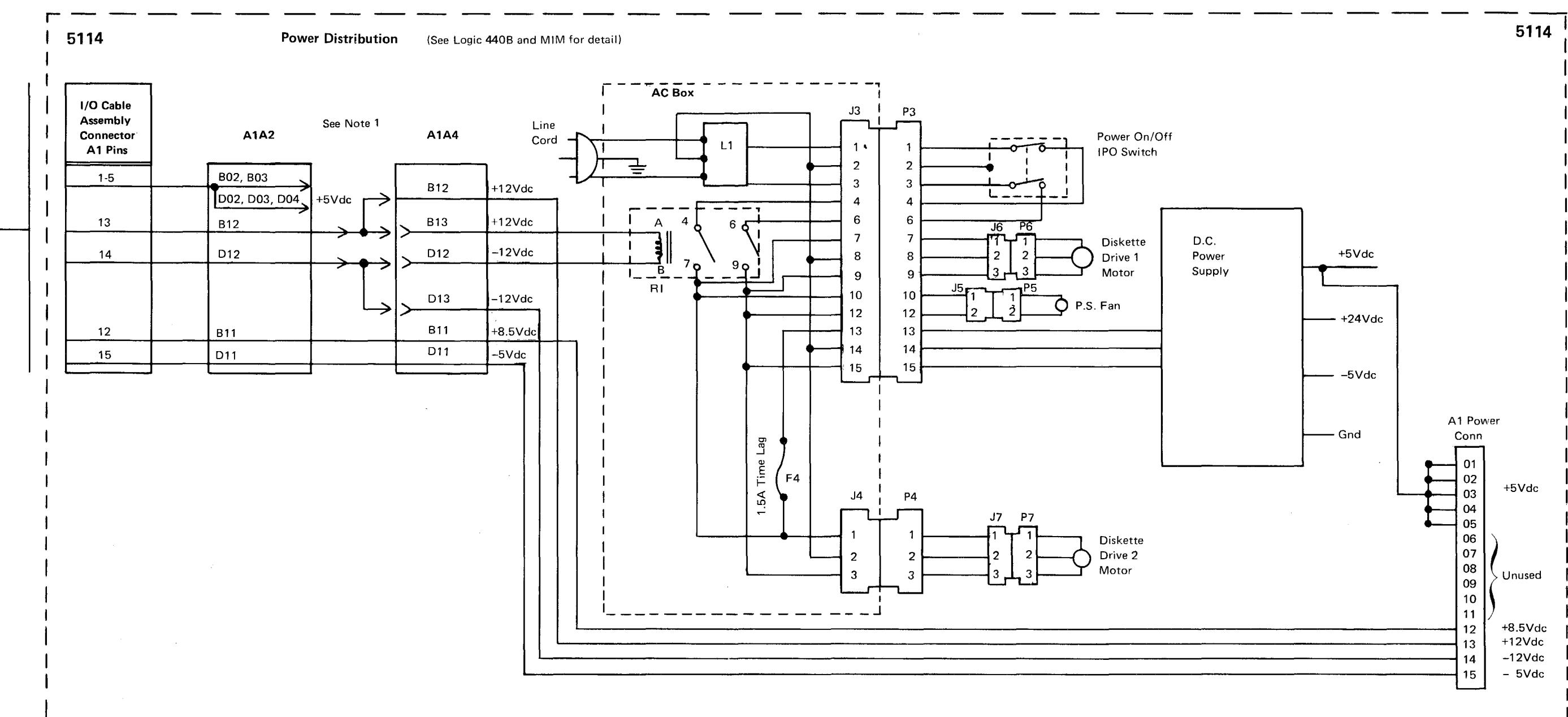


## BSCA/EIA 465



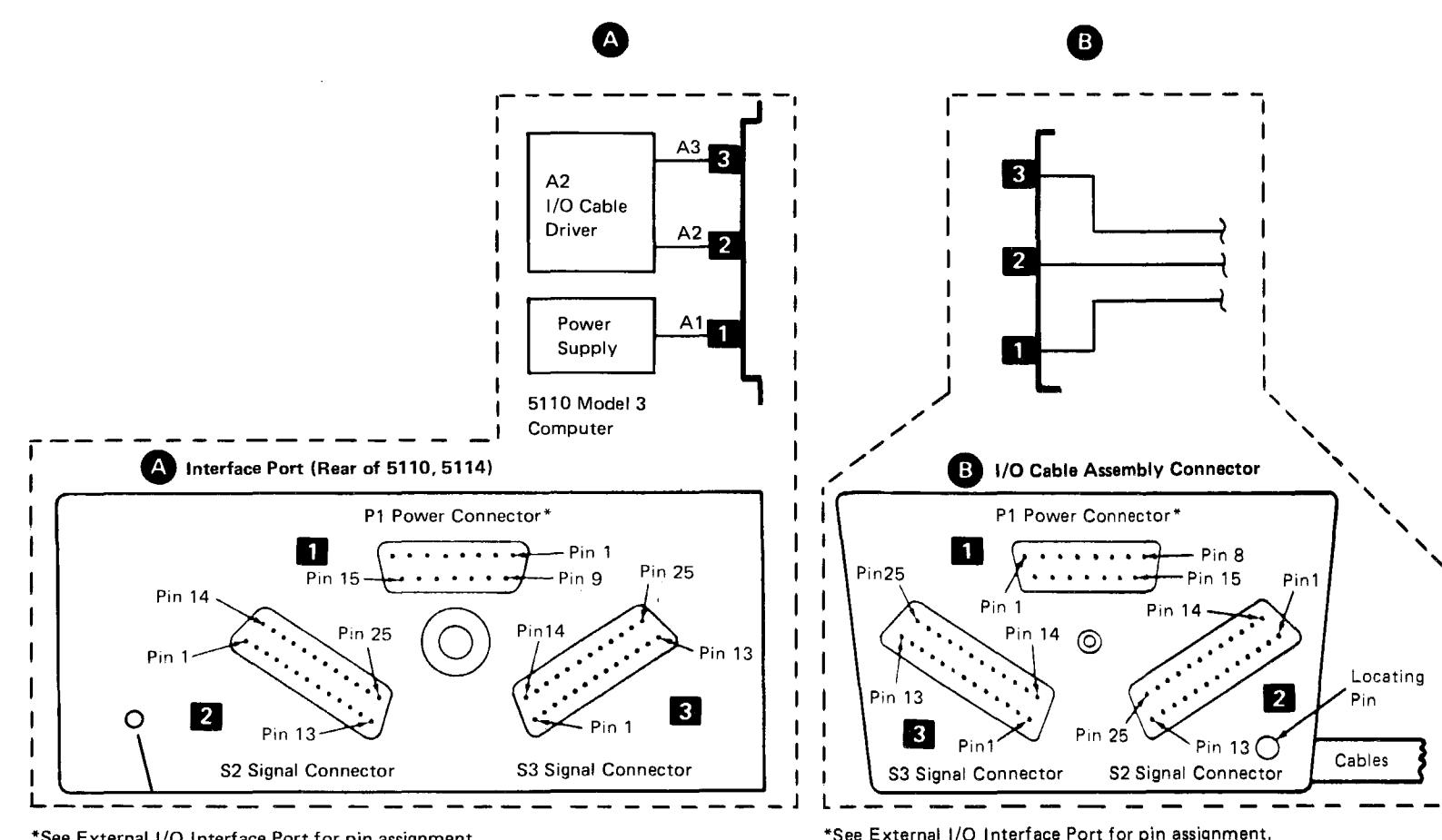
**5110 Model 3 480A  
AC Power Distribution**





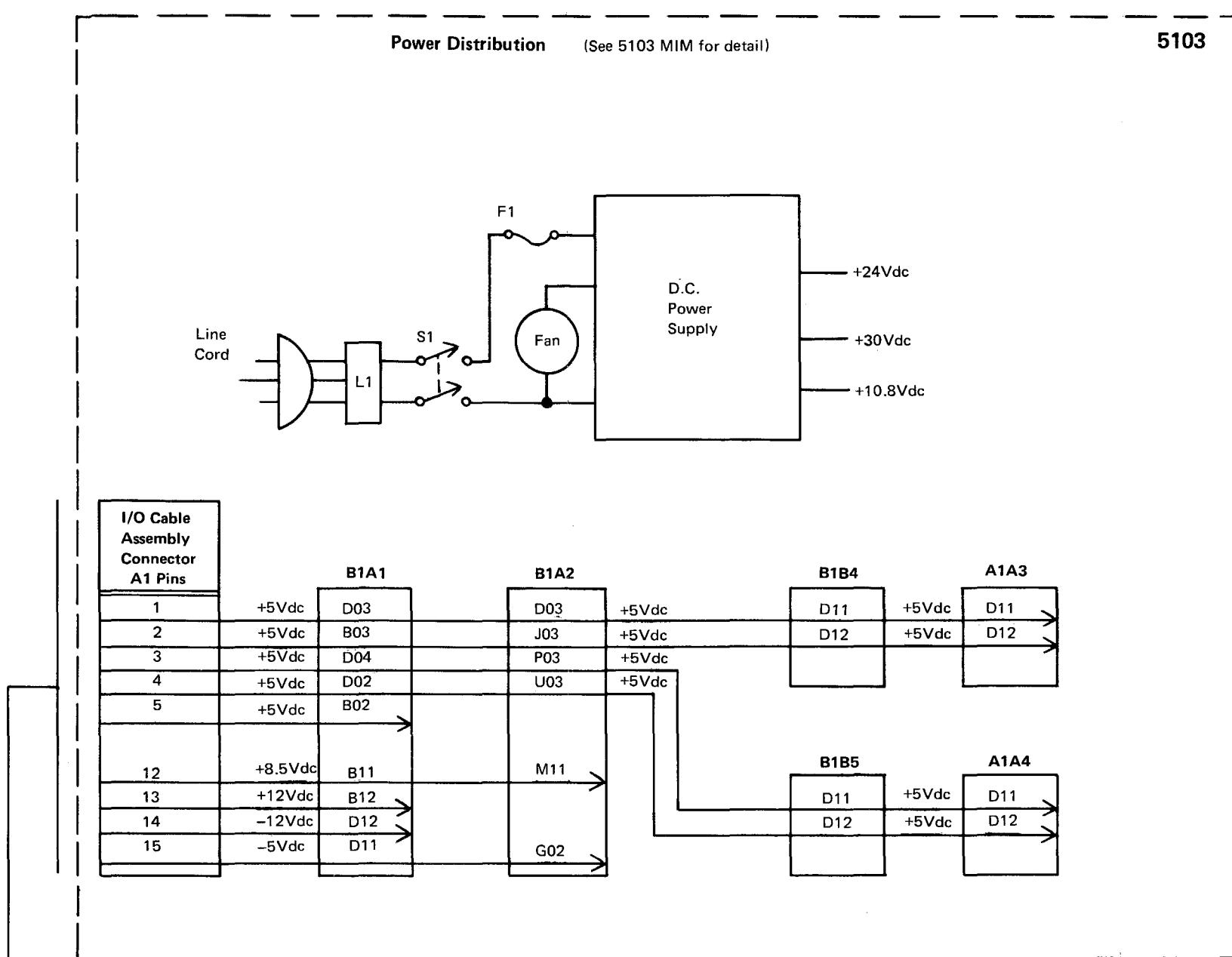
5110 I/O Interface Port  
A1 Power Connector  
(Logic 480B)

External I/O Interface Port	
A1 Power Conn	
Pin	Voltage
01	+5Vdc
02	+5Vdc
03	+5Vdc
04	+5Vdc
05	+5Vdc
06	Unused
07	Unused
08	Unused
09	Unused
10	Unused
11	Unused
12	+8.5Vdc
13	+12Vdc
14	-12Vdc
15	-5Vdc

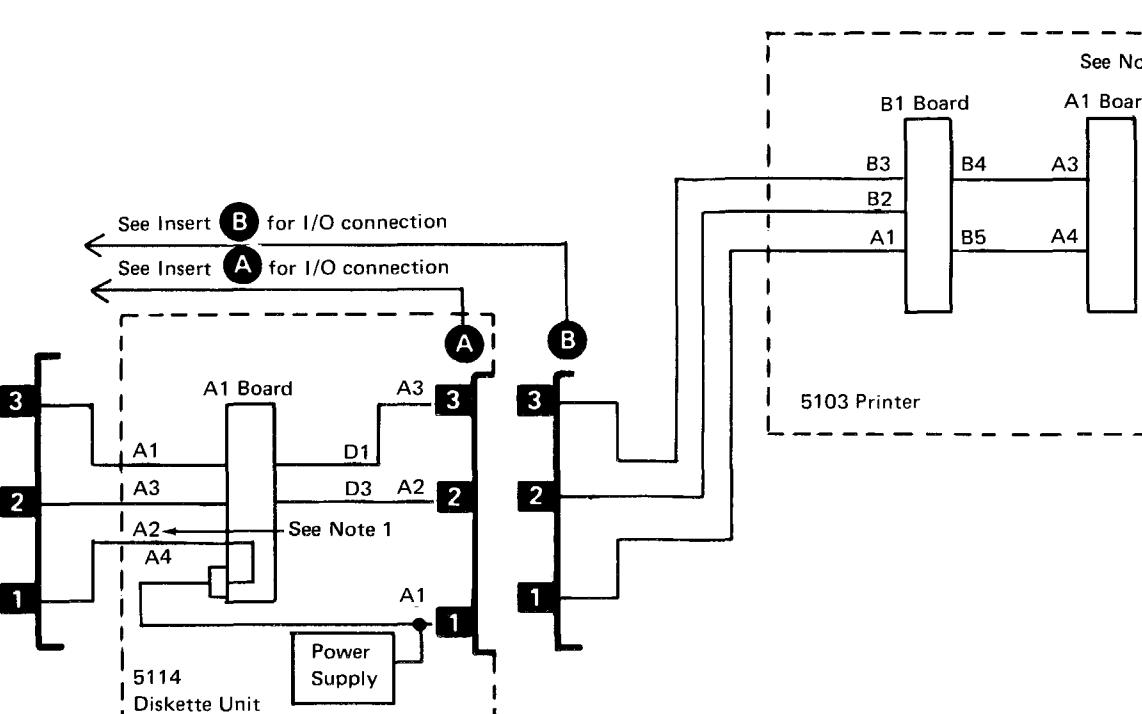


\*See External I/O Interface Port for pin assignment.

\*See External I/O Interface Port for pin assignment.



5103/5114 480C  
DC Power Distribution



Notes:

1. The 5110 +5Vdc stops here. The 5114 provides its own +5Vdc and +5Vdc for attaching devices. Also, ground is distributed via A2 and A3 connectors.
2. The cable terminator is permanently wired to the 5103 printer adapter card. If the printer is not in the system, a terminator must be installed on the last I/O device.

```
*****  
LINE NAME A2 A4 B2 C2 C4 D2 E4 F2 G2 H2 J2 K2 K4 L2 M2 CABLE  
*****  
+APL SWITCH  
+BUS IN BIT P D12 D12 M04 S12 S04 P04 Z3B03(H6B04)  
+BUS IN BIT P D02 D02 S02 S10 X2D12 X2D12  
+BUS IN BIT 0 D02 D02 S02 P12 D12 P12  
+BUS IN BIT 0 D02 D02 X4D12 X4D12  
+BUS IN BIT 1 D04 D04 P02 S03 U05 X4B10 X4B10  
+BUS IN BIT 1 D05 D05 G11 S04 P02 S02  
+BUS IN BIT 2 D05 D05 G11 S04 P02 S02  
+BUS IN BIT 2 D06 D06 S05 X4D13 X4D13  
+BUS IN BIT 3 D06 D06 S05 M05 S03  
+BUS IN BIT 3 D07 D07 J11 S07 M07 S04  
+BUS IN BIT 4 D07 D07 J11 S07 M07 S04  
+BUS IN BIT 4 D09 D09 S08 G11 S05  
+BUS IN BIT 5 D09 D09 S08 G11 S05  
+BUS IN BIT 5 D09 D09 X2D13 X2D13  
+BUS IN BIT 6 D10 D10 S09 P13 U02  
+BUS IN BIT 6 D11 D11 G10 S10 P10 U04  
+BUS IN BIT 7 D11 D11 G10 S10 P10 U04  
+BUS IN BIT 7 D21 D21 X4B07 X4B07  
+BUS OUT BIT P D21 D21 X2B10 X2B10  
*****
```

```
*****  
LINE NAME A2 A4 B2 C2 C4 D2 E4 F2 G2 H2 J2 K2 K4 L2 M2 CABLE  
*****
```

```
+BUS OUT BIT P G11 G11 J12 D02 D12 M04 J06  
-BUS OUT BIT 0 PWRD G10 G10 J10 B02 P06 J09 J07  
-BUS OUT BIT 1 PWRD G09 G09 B03 P09 G05 M03  
-BUS OUT BIT 2 PWRD G08 G08 B04 S06 J05 J02  
-BUS OUT BIT 4 PWRD G06 G06 B07 M04 G10 J09  
-BUS OUT BIT 5 PWRD G05 G05 B08 S10 G09 G10  
-BUS OUT BIT 6 PWRD G04 G04 J06 B09 M07 B13 J13  
-BUS OUT BIT 7 G03 G03 J07 B10 M07 G12 J10  
-BUS OUT BIT 3 G07 G07 B05 P11 J10 J05  
+CONTROL_STROBE_PWRD B12 B12 M09 B13 G12 B11 M04  
+C1_PWRD S07 G03 S02  
+C2_PWRD G04 J05 U04  
+C4_PWRD D12 P04 S07  
+C5_PWRD J04 P07 U11  
+DEVICE_ADDR_X0 X2B05 X2B05  
+DEVICE_ADDR_X0_PWRD B03 B03 M08 D04 G04 D07 X2B08 X2B08  
+DEVICE_ADDR_X1 B04 B04 P07 D05 B02 B07 X2D04  
+DEVICE_ADDR_X2_PWRD B05 B05 U09 D06 J06 D09 G07  
*****
```

```
*****  
LINE NAME A2 A4 B2 C2 C4 D2 E4 F2 G2 H2 J2 K2 K4 L2 M2 CABLE  
*****
```

```
+DEVICE_ADDR_X3 B06 B06 U12 D07 G07 D02 G13  
+DEVICE_ADDR_X3_PWRD B06 B06 U12 D07 G07 D02 G13  
+DEVICE_ADDR_Y0 B07 B07 S08 D09 M11 B09 G05  
+DEVICE_ADDR_Y0_PWRD B07 B07 S08 D09 M11 B09 G05  
+DEVICE_ADDR_Y1 B08 B08 M06 D10 G06 D10 G08  
+DEVICE_ADDR_Y1_PWRD B08 B08 M06 D10 G06 D10 G08  
+DEVICE_ADDR_Y2 B09 B09 M07 D11 U07 B10 M10  
+DEVICE_ADDR_Y2_PWRD B09 B09 M07 D11 U07 B10 M10  
+DEVICE_ADDR_Y3 B10 B10 U10 D12 U04 D11 G12  
+DEVICE_ADDR_Y3_PWRD B10 B10 U10 D12 U04 D11 G12  
+DEVICE_ADDRESS_Y1  
+EXT_HORIZ_DRIVE J05 U07 B09 Z3D11(J6E02)  
-GET_STROBE_PWRD B11 B11 G12 G12 B08 S13  
-INTERRUPT_1_REQ J02 X2D06 X2D06  
-INTERRUPT_1_REQ J02 X2D06 X2D06  
-INTERRUPT_2_REQ G12 J09 D13  
-INTERRUPT_2_REQ G12 J09 D13  
-MACHINE_CHECK J06 J06 M05 U12 U13 G06 S09 D06  
+MCC_3_PWRD  
+MCC_4  
*****
```

```
*****  
LINE NAME A2 A4 B2 C2 C4 D2 E4 F2 G2 H2 J2 K2 K4 L2 M2 CABLE  
*****
```

```
+MONITOR_VIDEO_OUT B13 B13 D09 B10  
+MONITOR_VIDEO_OUT B13 B13 D09 B10 Z3B13(K6B04)  
+OP_CODE_E_PWRD D13 D13 D13 M06 B10  
+OSC_PWRD  
+POWER_ON_RESET_PWRD J02 J02 S10 S13 M12 D09 B11 M02 Z4B07(K6B02)  
-PUT_STROBE_PWRD B13 B13 P09 G02 J12 B02  
-RESTART_SWITCH B13 B13 G02 D05 G06 P02 Z3D13(K6B02)  
-SELECT_ROS  
-SELECT_ROS  
+START_EXECUTE_PWRD J07 J07 U05 B12 D05 J12  
-STORAGE_ADDR_BIT_A_PWRD  
-STORAGE_ADDR_BIT_B_PWRD  
-STORAGE_ADDR_BIT_C_PWRD  
-STORAGE_ADDR_BIT_D_PWRD  
-STORAGE_ADDR_BIT_E_PWRD  
-STORAGE_ADDR_BIT_0 B06 G04 U04 G09 U10 B12  
-STORAGE_ADDR_BIT_0 X4B12 X4B12  
-STORAGE_ADDR_BIT_1 S04 G08 U09 B13  
-STORAGE_ADDR_BIT_1 S05 G07 U07 D11  
-STORAGE_ADDR_BIT_1 U05 J07 S07 D10  
-STORAGE_ADDR_BIT_1 U06 J06 M13 B09  
-STORAGE_ADDR_BIT_2 B06 G04 U06  
-STORAGE_ADDR_BIT_2 X4B12 X4B12  
-STORAGE_ADDR_BIT_3 S09 G13 U13  
-STORAGE_ADDR_BIT_3 X4B13 X4B13  
-STORAGE_ADDR_BIT_3 D05 J12 U12  
*****
```

```
*****  
LINE NAME A2 A4 B2 C2 C4 D2 E4 F2 G2 H2 J2 K2 K4 L2 M2 CABLE  
*****
```

```
*****  
LINE NAME A2 A4 B2 C2 C4 D2 E4 F2 G2 H2 J2 K2 K4 L2 M2 CABLE  
*****  
+APL SWITCH  
+BUS IN BIT P D12 D12 M04 S12 S04 P04 Z2B11 X2B11  
+BUS IN BIT P D02 D02 S02 S10 X2D12 X2D12  
+BUS IN BIT 0 D02 D02 S02 P12 D12 P12  
+BUS_IN_BIT_0 D02 D02 X4D12 X4D12  
+BUS_IN_BIT_1 D04 D04 P02 S03 U05 X4B10 X4B10  
+BUS_IN_BIT_1 D05 D05 G11 S04 P02 S02  
+BUS_IN_BIT_2 D05 D05 G11 S04 P02 S02  
+BUS_IN_BIT_2 D06 D06 S05 X4D13 X4D13  
+BUS_IN_BIT_3 D06 D06 S05 M05 S03  
+BUS_IN_BIT_3 D07 D07 J11 S07 M07 S04  
+BUS_IN_BIT_4 D07 D07 J11 S07 M07 S04  
+BUS_IN_BIT_5 D09 D09 S08 G11 S05  
+BUS_IN_BIT_5 D09 D09 X2D13 X2D13  
+BUS_IN_BIT_6 D10 D10 S09 P13 U02  
+BUS_IN_BIT_7 D11 D11 G10 S10 P10 U04  
+BUS_IN_BIT_7 D21 D21 X4B07 X4B07  
+BUS_OUT_BIT_P D21 D21 X2B10 X2B10  
*****
```

```
+STORAGE_ADDR_BIT_2 D07 B05 J13 U11 G08  
-STORAGE_ADDR_BIT_2 PWRD B05 J13 U11 G08  
-STORAGE_ADDR_BIT_3 B05 J13 U11 G08  
-STORAGE_ADDR_BIT_3 PWRD B05 J13 U11 G08  
-STORAGE_ADDR_BIT_3 PWRD B05 J13 U11 G08  
-STORAGE_ADDR_BIT_4_PWRD D04 G12 S13  
-STORAGE_ADDR_BIT_5 B11 B07 G11 S12  
-STORAGE_ADDR_BIT_6 B10 B09 J11 P10  
-STORAGE_ADDR_BIT_7_PWRD D13 J10 S10 J06  
-STORAGE_ADDR_BIT_8_PWRD D09 J09 S09 G05  
-STORAGE_ADDR_BIT_9_PWRD S03 G10 S08 G04  
-STORAGE_R/W_BUS_BIT_P_EVEN D11 B07 G11 S12  
-STORAGE_R/W_BUS_BIT_P_EVEN B10 B09 J11 P10  
-STORAGE_R/W_BUS_BIT_P_ODD J06 B13 B13 B02  
+STORAGE_R/W_BUS_BIT_0_EVEN S05 P02 D02 J12  
+STORAGE_R/W_BUS_BIT_0_EVEN S02 S02  
+STORAGE_R/W_BUS_BIT_0_ODD U05 G07 B07 D10 B07  
+STORAGE_R/W_BUS_BIT_0_ODD U06 M06  
+STORAGE_R/W_BUS_BIT_1_EVEN U12 P13 D04 D04 J11  
+STORAGE_R/W_BUS_BIT_1_EVEN U11  
*****
```

```
*****  
LINE NAME A2 A4 B2 C2 C4 D2 E4 F2 G2 H2 J2 K2 K4 L2 M2 CABLE  
*****  
+STORAGE_R/W_BUS_BIT_1_ODD M08 J07 B08 D12 D07  
+STORAGE_R/W_BUS_BIT_1_ODD M07  
+STORAGE_R/W_BUS_BIT_2_EVEN S07 M12 B04 B04 J09  
+STORAGE_R/W_BUS_BIT_2_EVEN P06  
+STORAGE_R/W_BUS_BIT_2_ODD S11 G05 D07 D13 B08  
+STORAGE_R/W_BUS_BIT_2_ODD P09  
+STORAGE_R/W_BUS_BIT_3_EVEN S12 M05 B05 J07  
+STORAGE_R/W_BUS_BIT_3_EVEN M09  
+STORAGE_R/W_BUS_BIT_3_ODD S08 J13 G02 G02 D04  
+STORAGE_R/W_BUS_BIT_3_ODD P12  
+STORAGE_R/W_BUS_BIT_4_EVEN U06 U02 D05 B02 J05  
+STORAGE_R/W_BUS_BIT_4_EVEN U12  
+STORAGE_R/W_BUS_BIT_4_ODD M13 J12 G03 G03 B05  
+STORAGE_R/W_BUS_BIT_4_ODD M08  
+STORAGE_R/W_BUS_BIT_5_EVEN P12 M13 D06 B03 J04  
+STORAGE_R/W_BUS_BIT_5_EVEN S12  
+STORAGE_R/W_BUS_BIT_5_ODD U09 J09 D12 G04 B04  
+STORAGE_R/W_BUS_BIT_5_ODD P04  
+STORAGE_R/W_BUS_BIT_6_EVEN P10 P07 B02 B08 D12  
+STORAGE_R/W_BUS_BIT_6_EVEN P11  
*****
```

```
*****  
LINE NAME A2 A4 B2 C2 C4 D2 E4 F2 G2 H2 J2 K2 K4 L2 M2 CABLE  
*****  
+STORAGE_R/W_BUS_BIT_6_ODD U10 G10 D13 J04 D02  
+STORAGE_R/W_BUS_BIT_6_ODD M03  
+STORAGE_R/W_BUS_BIT_7_EVEN S09 M10 B03 B09 D13  
+STORAGE_R/W_BUS_BIT_7_EVEN S04  
+STORAGE_R/W_BUS_BIT_7_ODD U11 G13 B12 B12 D06  
+STORAGE_R/W_BUS_BIT_7_ODD M04  
+WRITE_EVEN_TIMED U07 J11 J02  
+WRITE_ODD_TIMED B08 J12 J10  
*****
```

Note:  
This net listing does not contain  
any 1 or 2 pin nets.

5110 Model 3 485  
A1 Board Net Listing